ABSTRACT OF THE DISCLOSURE

According to various aspects and embodiments of this invention, a semiconductor device having many pins can effectively be tested using a test system having fewer pins. A semiconductor device test system and method are provided to effectively test a semiconductor device having many pins. The test system includes a pin electronics (PE) card and a pattern memory. The PE card preferably includes a plurality of comparator and driver units, wherein each comparator and driver unit can include a driver for driving a predetermined input signal pattern to be applied to an input pin of the semiconductor device and a comparator for comparing data output from an output pin of the semiconductor device with a predetermined output signal pattern. Some or all of the pins of the semiconductor device are divided into pin groups having K number of pins. The PE card also preferably includes a plurality of control units for electrically connecting each of the comparator and driver units to a selected pin in a selected pin group of the semiconductor device in response to a control signal. A pattern memory can be used to store input signal patterns and output signal patterns.